From Vacuum Tubes to Nanotechnology: Past, Present and Future

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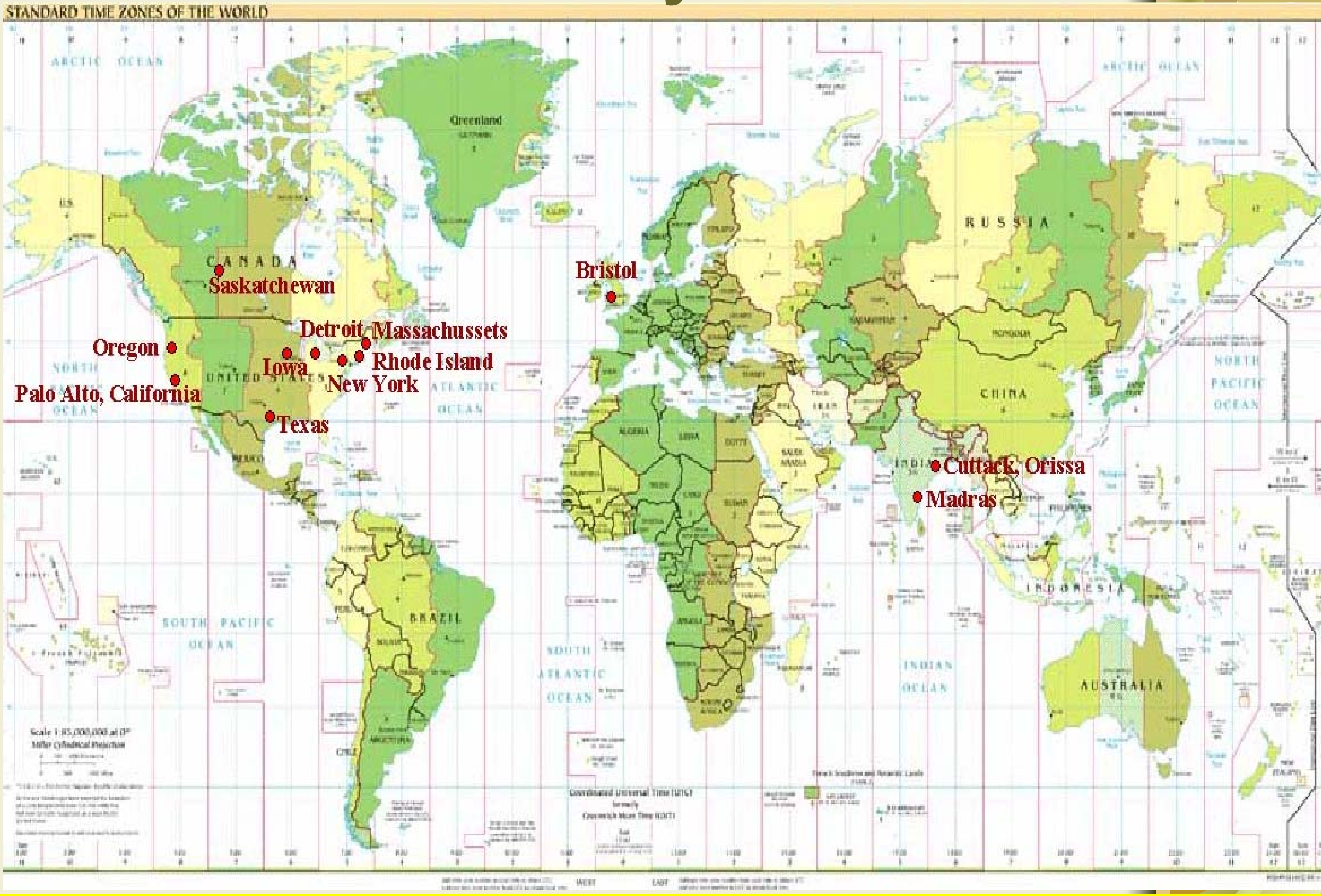
Place lived over the years



Mechanical Computers (1642-1945)

- Calculating Machine by Blaise Pascal (1623-1662)
- After 150 years Charles Babbage (1792-1871) invented speedometer
- Konrad Zuse (1930) built a series of automatic calculating machine
- Aiken’s first machine, the Mark I, was completed at Harvard in 1944

After that the electronic era had begin

ENIAC – Background (1943-1946)

- ENIAC: Electronic Numerical Integrator And Computer
- University of Pennsylvania (USA)
- Eckert and Mauchly
- Trajectory tables for weapons (war effect)
- Started 1943
- Finished 1946

war effort

until 1955

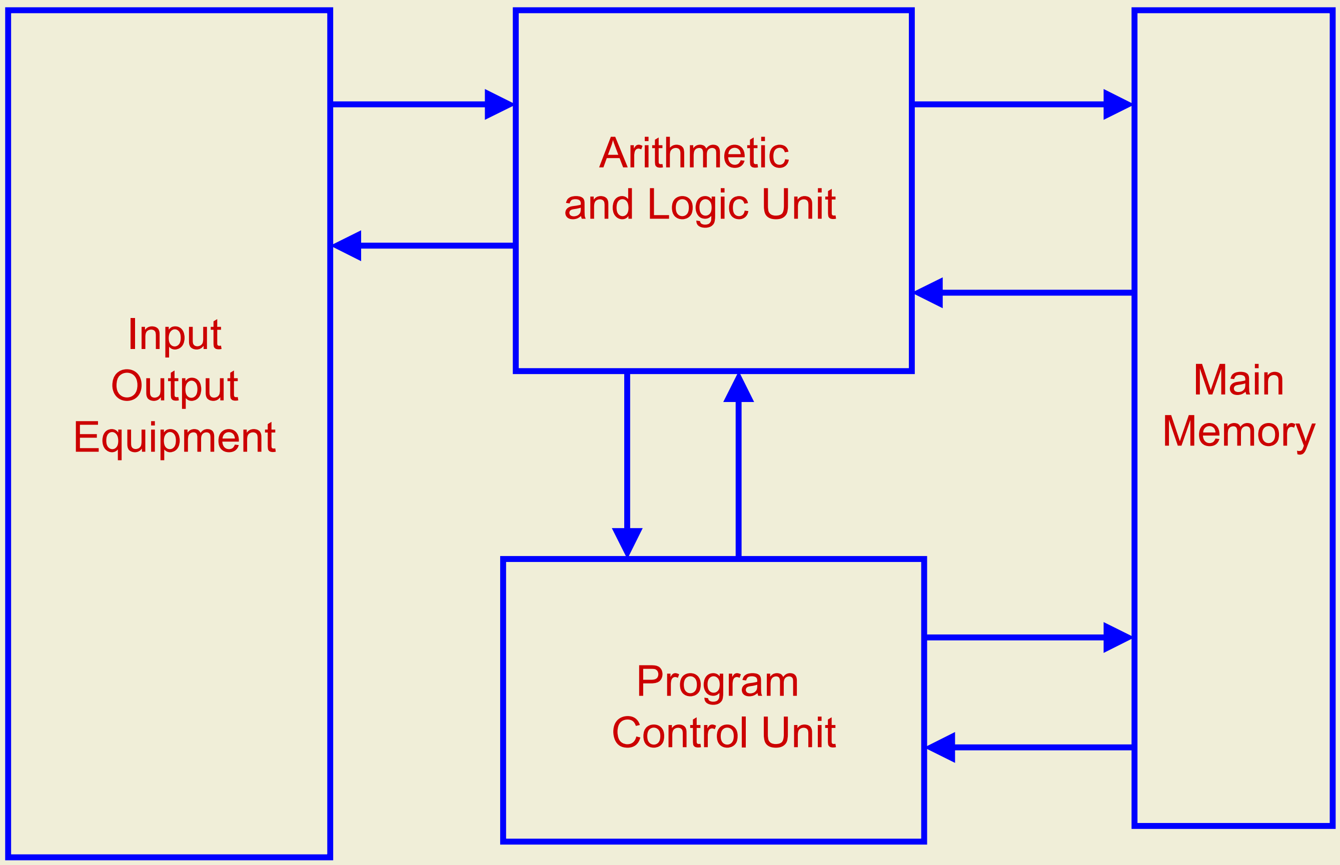
ENIAC – Details (1943-1946)

- Decimal (not binary)
- 20 accumulators of 10 digits
- Programmed manually by switches
- **18,000** vacuum tubes
- 30 tons
- 15,000 square feet
- **140 kW** power consumption
- 5,000 additions per second

Von Neumann / Turing (1952)

- Stored Program concept
- Main memory storing programs and data
- ALU operating on binary data
- Princeton Institute for Advanced Studies
  - IAS
- Completed 1952
- The basic architecture still survives

Von Neumann Machine (1952)



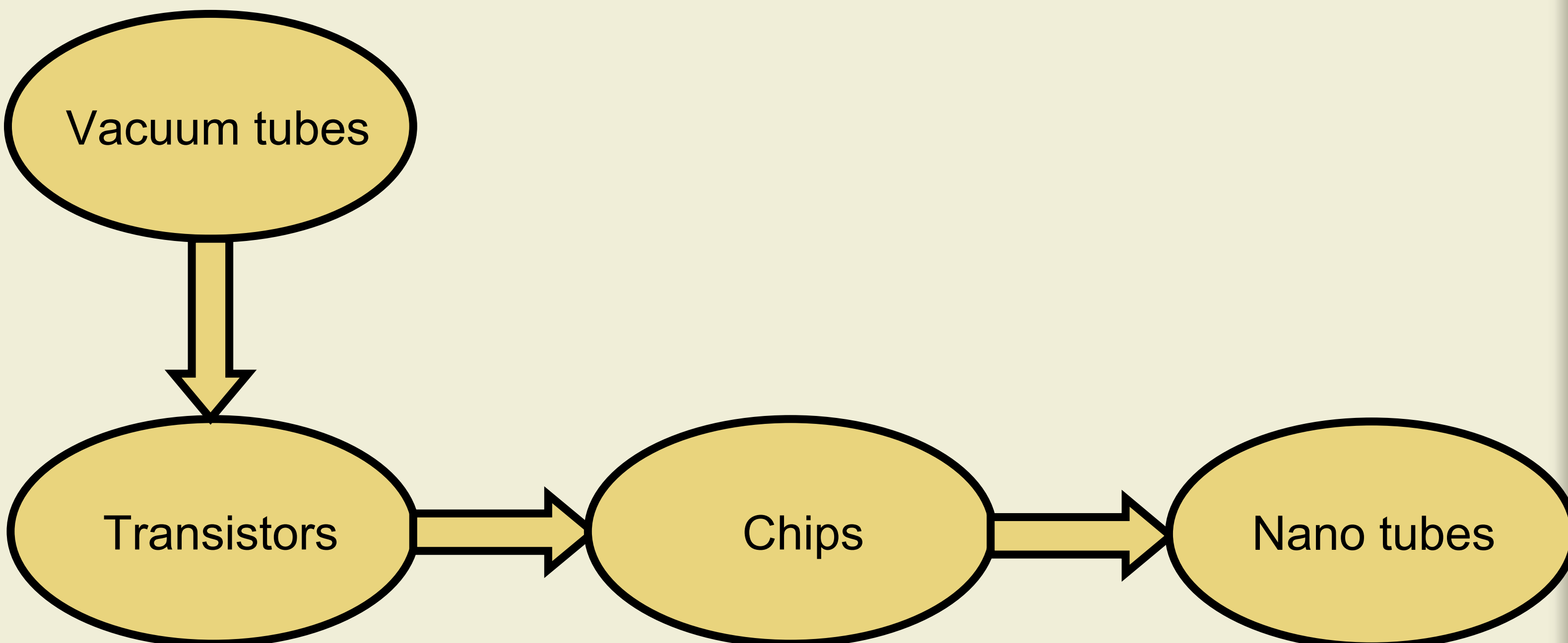
What Has Really Happened ?

THE WORLD IS STILL THE SAME

The PC is the same old Von Neumann

What has really changed

Technology



Transistors (1955-1965)

- Replaced vacuum tubes
- Smaller
- Cheaper
- Less heat dissipation
- Solid State device
- Made from Silicon (Sand)
- Invented 1947 at Bell Labs by William Shockley et al.
- Not Patented

Transistor Based Computers 1955-1965

- Second generation machines
- NCR & RCA produced small transistor machines
- IBM 7000
- DEC - 1957
  - Produced PDP-1
  - Referred to as minicomputers fashioned after miniskirt

Microelectronics (1965-1970)

- Literally - “small electronics”
- A computer is made up of gates, memory cells and interconnections
- These can be manufactured on a semiconductor
  - e.g. silicon wafer
- Availability of hand held calculators

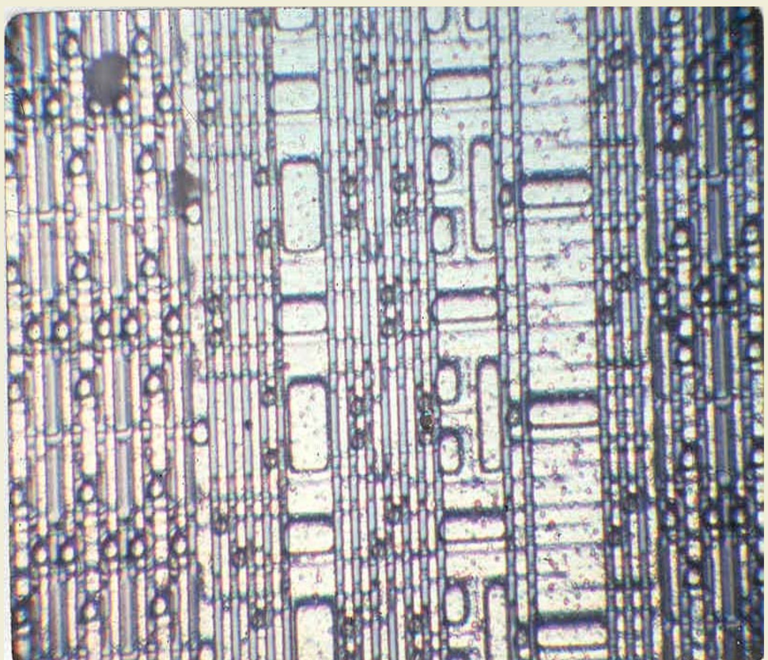
Generations of Computer

- Vacuum tube - 1946-1957
- Transistor - 1958-1964
- Small scale integration - 1965 on
  - Up to 100 devices on a chip
- Medium scale integration - to 1971
  - 100-3,000 devices on a chip
- Large scale integration - 1971-1977
  - 3,000 - 100,000 devices on a chip
- Very large scale integration - 1978 to 2004
  - 100,000 - 100,000,000 devices on a chip
- Ultra large scale integration – 2004 onwards
  - 100 million - 1 billion devices on a chip

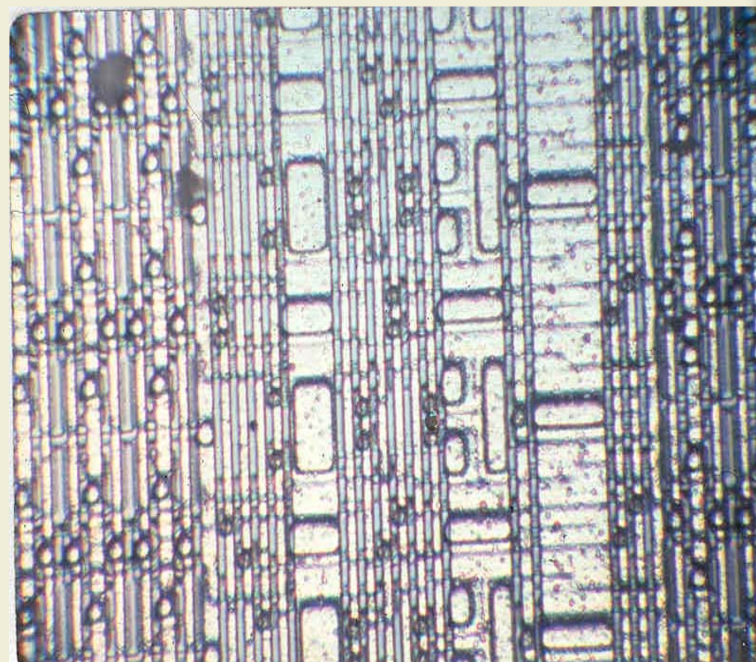
1978-Hello Silicon Valley

- Hot new technology
  - 3μ nMOS μ = 10^{-6} meter
  - The width of lines called feature size
  - Grid of interconnections

HMOS-2147 at Intel



VMOS at AMI



The Roaring 80's and 90's

- Silicon Valley was booming
  - Some faculty took leave to start companies
  - Many of my students joined and some started one
  - Kumar Ganapati sold his company for 500 million in 2000
- Workstation were invented
  - Apollo, Sun, SGI
- Birth of Modern CAD
  - Daisy, Mentor, Valid, Origins of Cadence

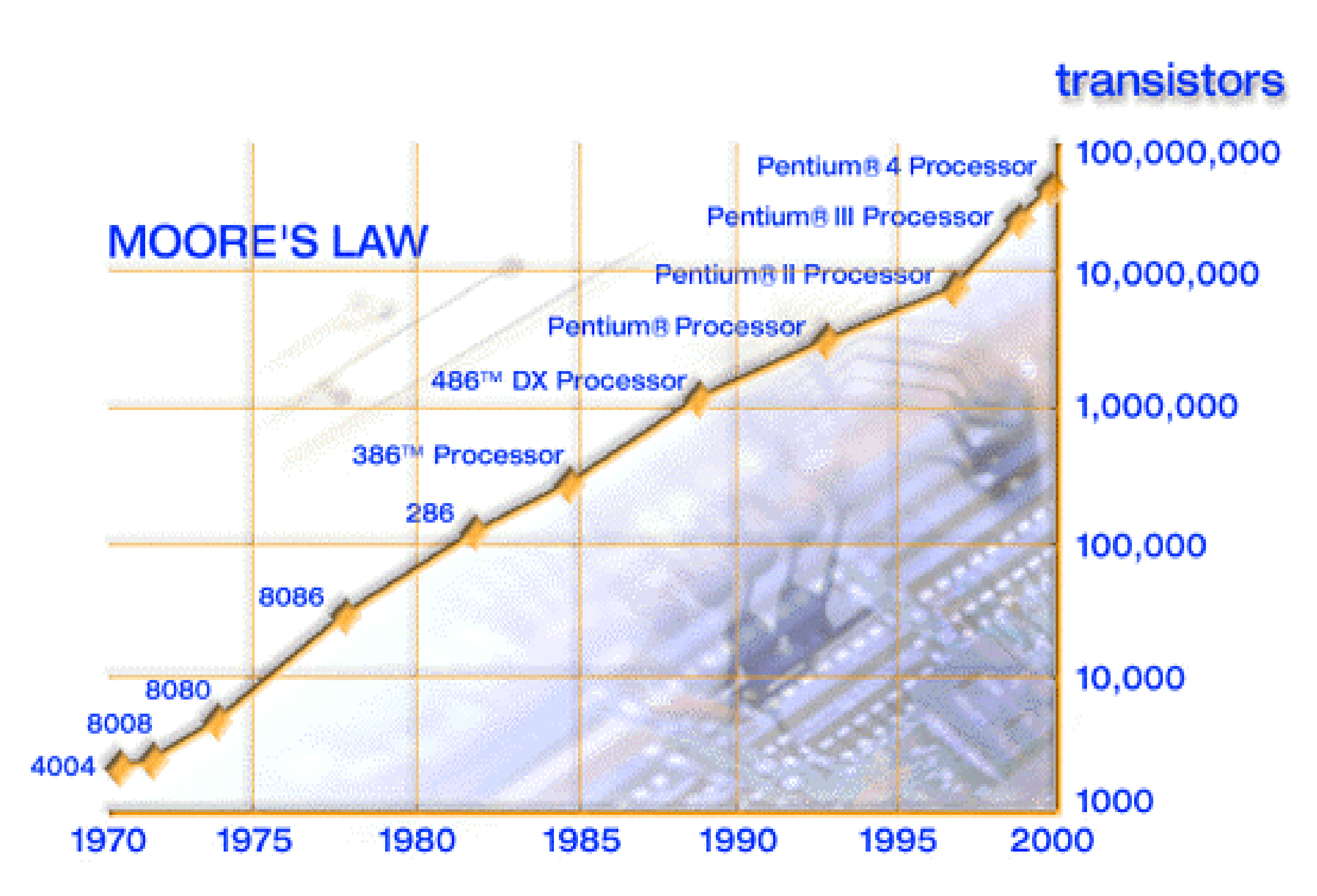
Intel - Pentium

- 1985 - 80386 (16-33MHz) SX and DX
  - 32-bit, 275,000 transistors
- 1989 - 80486(25-50MHz) SX and Dx
  - 32-bit data width, 1.2 million transistors
- 1993 - Pentium(60-166MHz)
  - 32-bit/32-bit bus, 3.1 million transistors
- 1995 Pentium Pro, 1997 Pentium II,
- 1999 Pentium III, Merced(IA-64)
- 2000 Pentium IV
- 2004 Pentium IV Prescott
  - First nanoproduct

Moore's Law

- Increased density of components on chip
- Gordon Moore - cofounder of Intel
- Number of transistors on a chip will double every year (now every three years)
- Since 1970's development has slowed a little
  - Number of transistors doubles every 18 months
  - Last few years more like every 3 years

Contd



The Pentium 4 contains 54 million transistors
The Prescott Pentium 120 million (2004)

Number of Devices on Chip

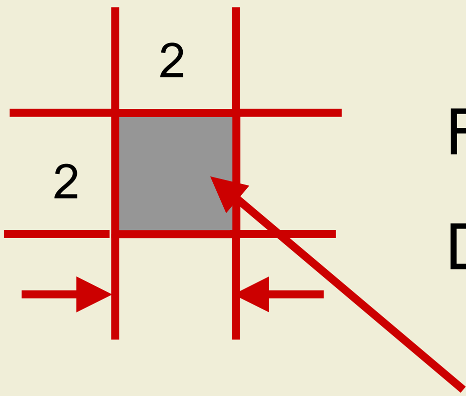
- Two ways to increase
  - Reduce Feature Size
  - Increase Chip Area
- Reduction of feature size
  - Yield Problem
    - More defects
  - Noise Problem Voltage levels have to be reduced
    - Manufacturing problems

Technology Scaling

Seems simple,

- Every 1*, 1.5*, 2
  - Number of transistors double
  - Transistors gets faster
  - Gates becomes lower power (CMOS)
- Life just gets better and better ?

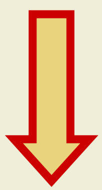
Scaling (Reduction Feature Size)

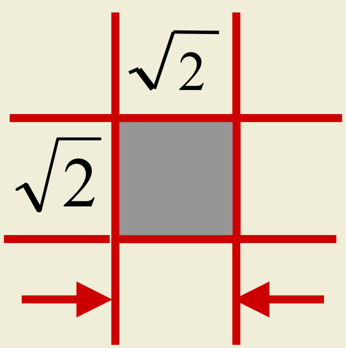


Feature size = 2

Device size = 4

Transistor area





To double the number of devices

Feature size = $\sqrt{2}$

Device size = 2

How long is a nanometer ?

New feature sizes are now in nanometers

- A nanometer is about 100,000 times smaller than the diameter of a human hair

>*object*	*characteristic size*
person	1 m
grain of sand	1 mm
human hair (thickness) .	1 mm = 100 µm
red blood cell	10 µm
wavelength of light	1 µm = 10^+3 nm
virus	100 nm
atom	.1 nm
1 µm	1000 nm
1 µm	10^{-6} m

Future Feature Sizes

90 Nanometer (2004) Intel Pentium Prescott

$$\frac{90}{\sqrt{2}} \approx 64$$

(approx 2006)

$$\frac{64}{\sqrt{2}} \approx 45$$

(approx 2008)

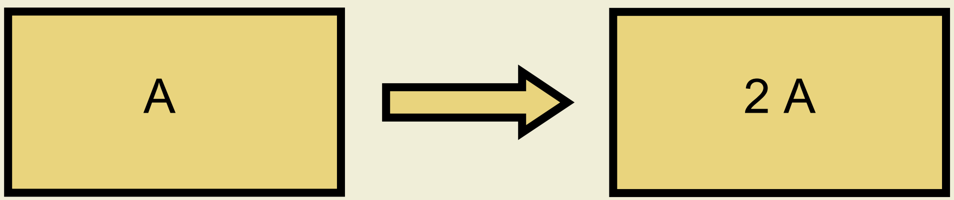
Problems

- Every reduction feature size requires 2 X investment in Research and Development
- Depends on economy
- Slow down in last few years in Moore’s law

Alternative solution (Increase the Chip Area)

Doubling the area to double the number of devices

- Yield Problem (Mayor and Pradhan: Centre satellite model)



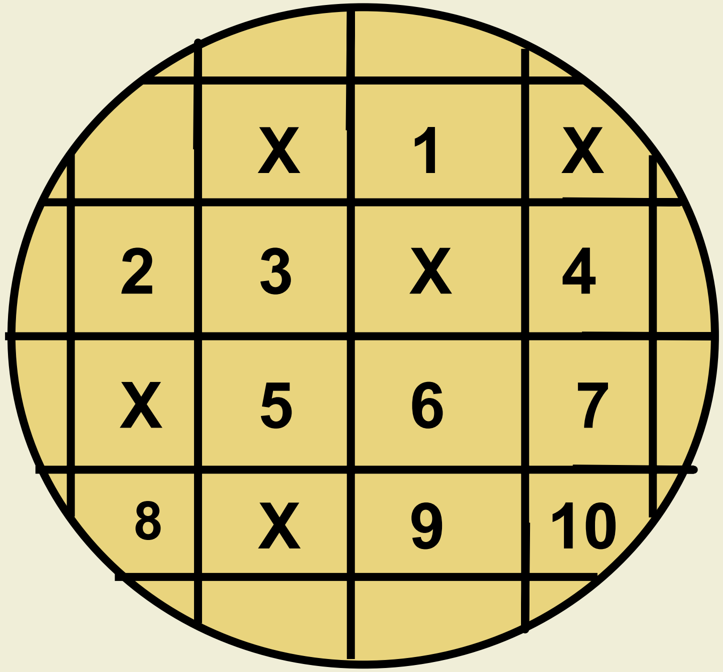
$$Y = e^{-\lambda A} \qquad Y = e^{-2\lambda A}$$

λ = defect density

The new yield is lower by 90 % of the original yield

- Power problem
  - Wafer scale integration
    - Trilogy Spectacular Failure in the 80's
      - 1 KW per wafer

The Yield Problems

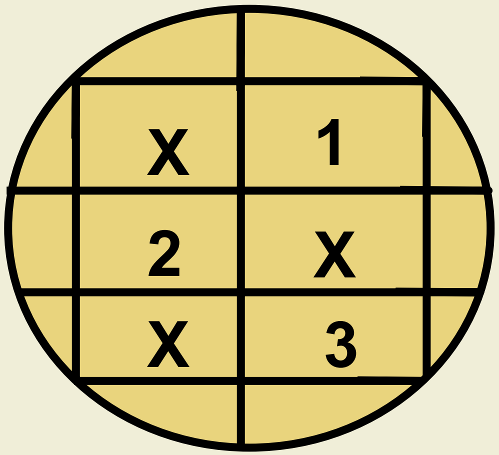


X = Defective

Wafer

- Large number of defective chips on a wafer
- Number of useful chips = 10 out of 15

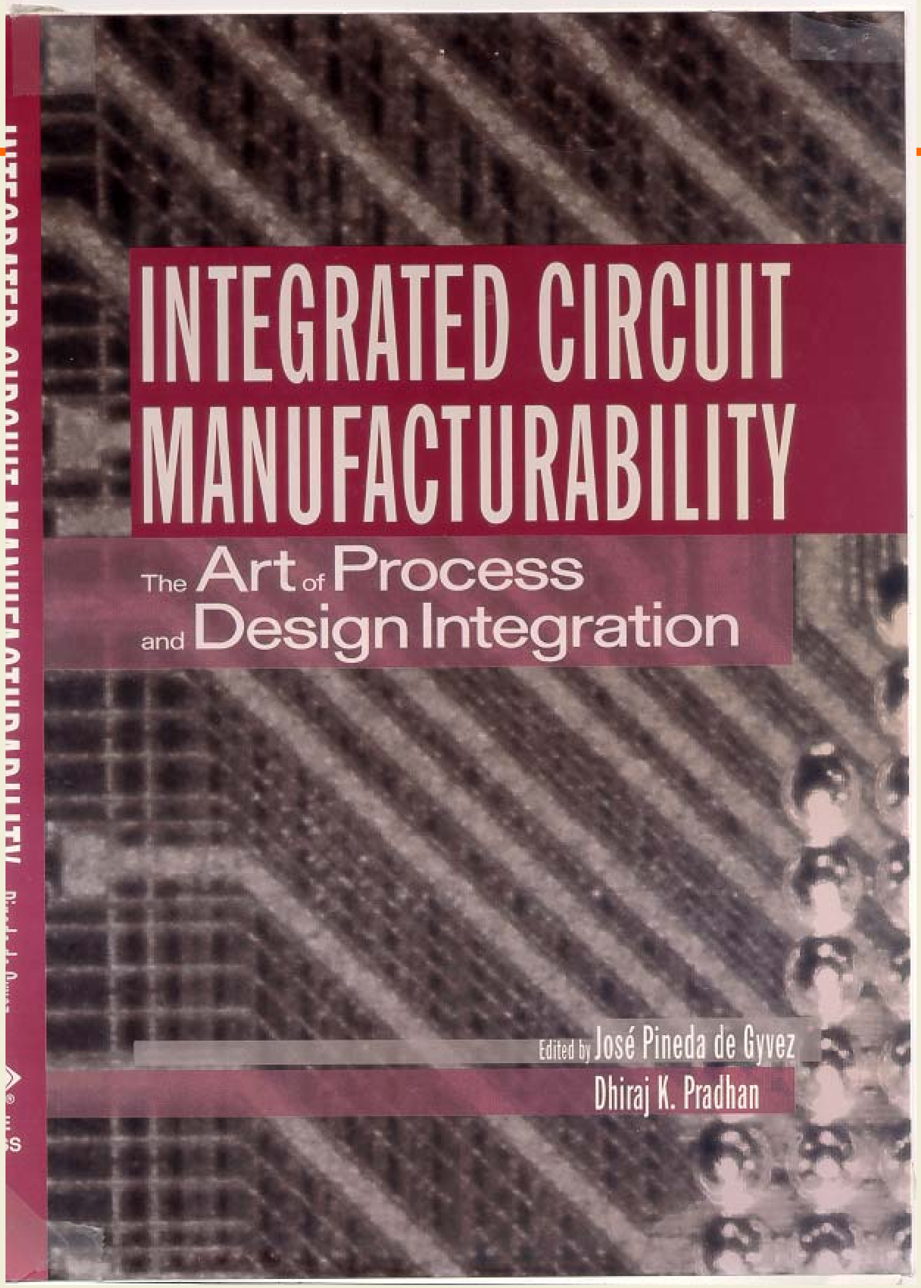
Increasing Area



- Doubling the size of chips for doubles the number of devices
  - Number of useful chips = 3 out of 6
- However these will be more defects because the probability of defects increased by e^2
- Cost will increase 900 %

Solution to Future Yield Problems

Nano Technology will require
Defect Tolerant Chips

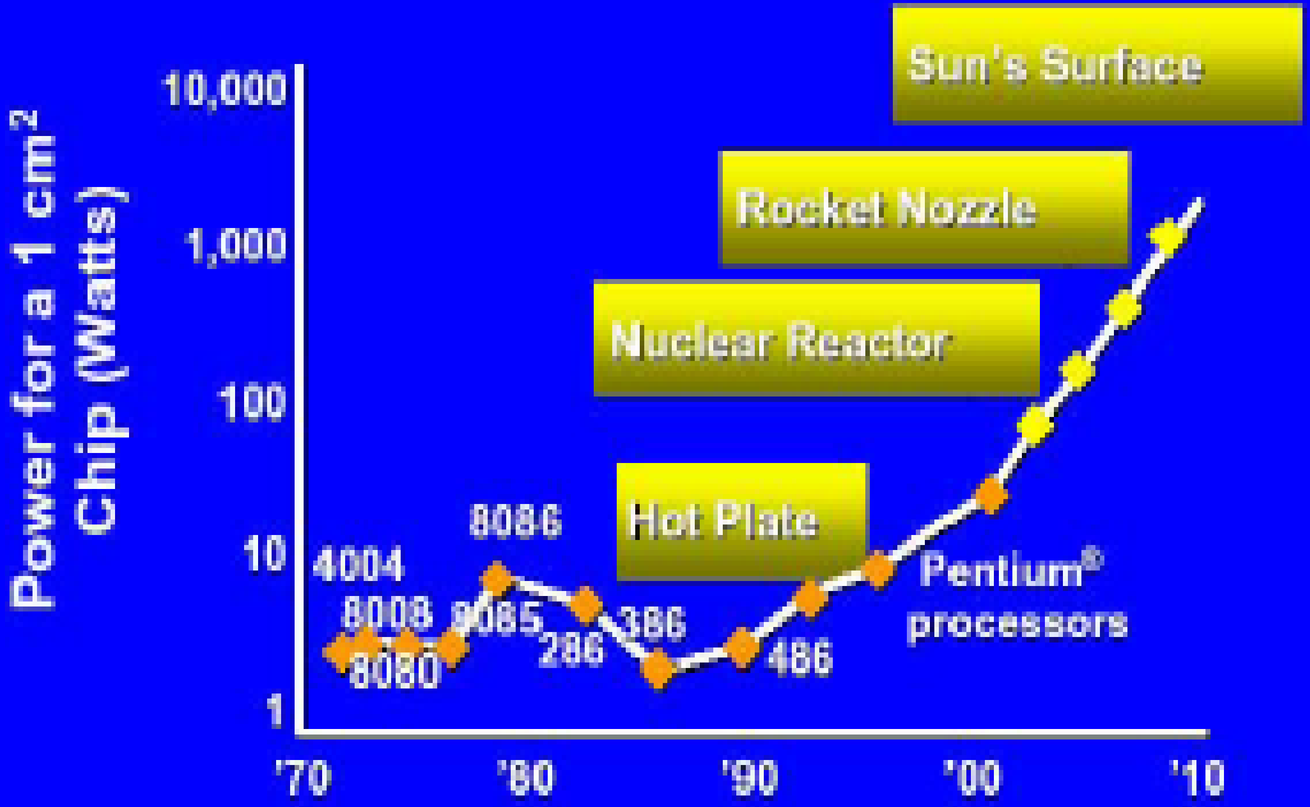

INTEGRATED CIRCUIT MANUFACTURABILITY
The Art of Process and Design Integration
Edited by José Pineda de Gyvez
Dhiraj K. Pradhan

Problem We are Facing Today

- Power dissipation
- Design cost
- What to do with all the functionality possible

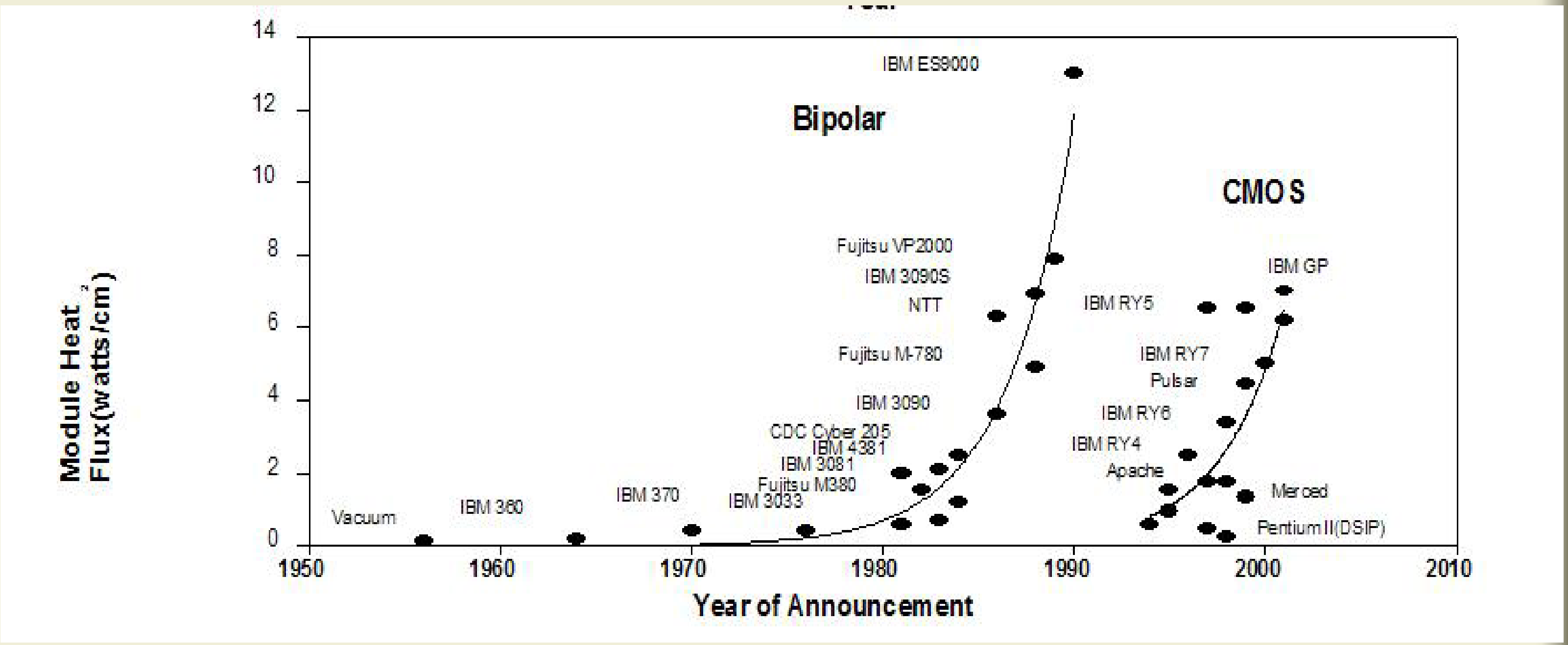
Guess that is why people listen to Moore…

Power Extrapolation



The Power Problem

- Until mid 80s technology was mixed
  - nMOS, bipolar, some CMOS
- Power really forced the issue
  - nMOS, bipolar gates dissipate static power

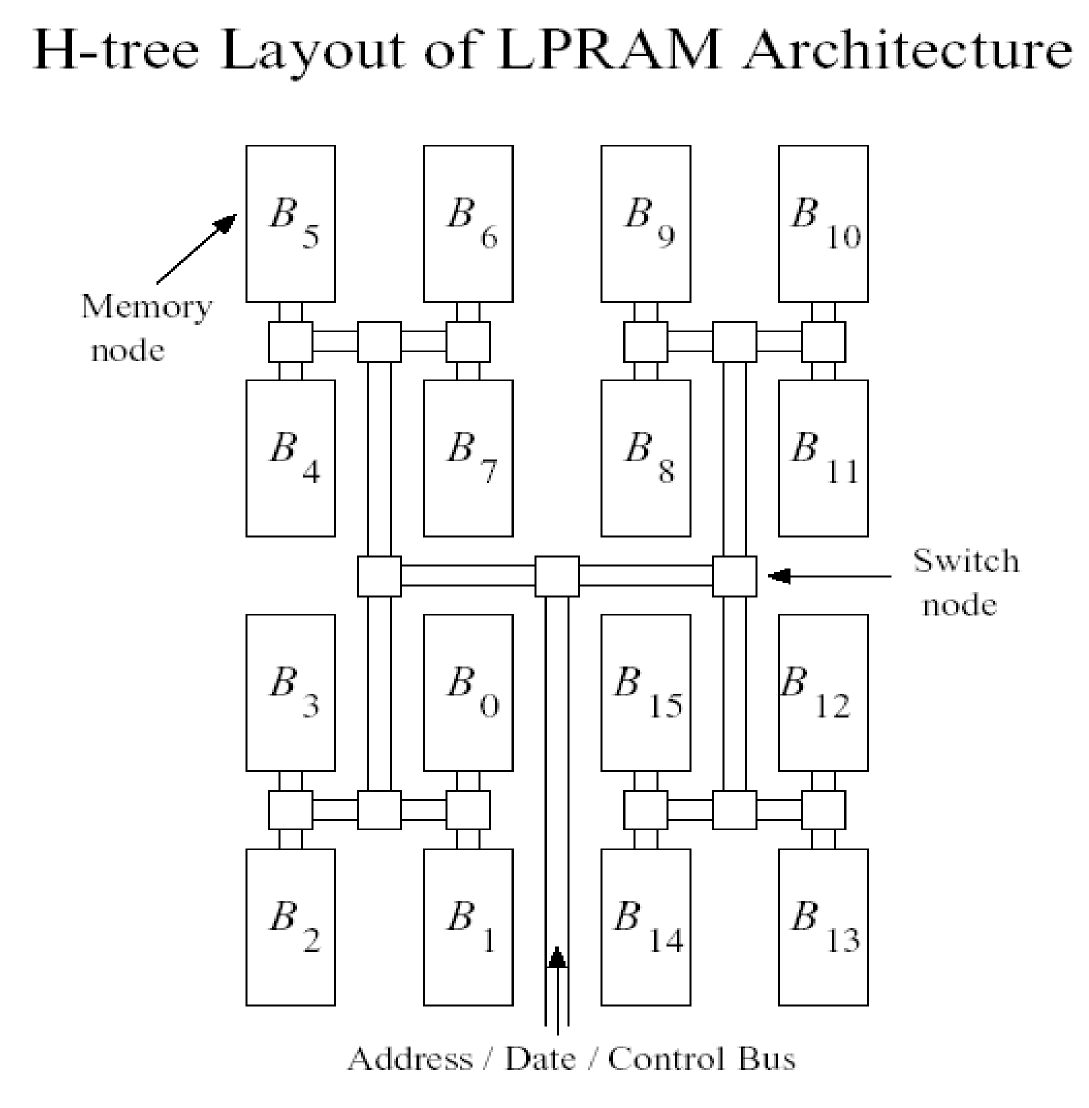


Need for low power

Sales

- 400 million mobile phones/year
- 40 million automobiles/year
- Price of computers have been drastically reduced:
  - Performance scaling due to number of devices on a chip.
- If automobile technology had undergone the same then we should be buying a Mercedez for less than a £
- Batteries have not scaled so we are in a box.

Bristol RAM (Patent pending)



Proposed Solution

- Architectural high level solution
- Power reduction with improved performance and test
- Normal operational power reduction
- Test operational power reduction
- Allows tradeoff between area, power and performance
- 30 to 60% Power Reduction

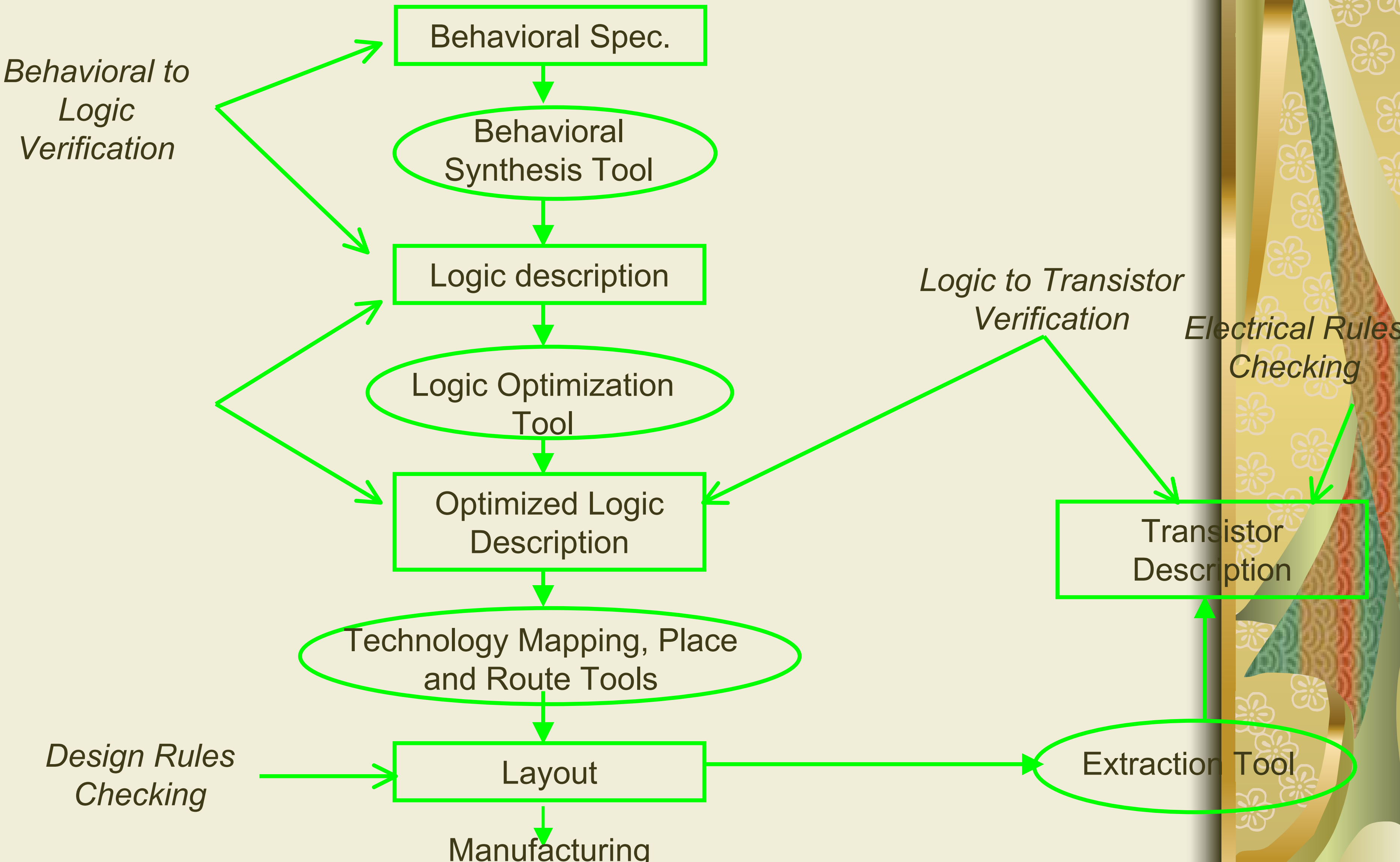
What About Leakage

- Great fear about leakage currents
  - Recently it has been rising exponentially
  - Current high-power chips have 40A leakage
- Need new materials (Intel)

The New Reality

- We are no-longer device limited
  - Don't generally need more gates
- We have become power limited
  - Easy to build chip that exceeds power budget
    Added more levels of metal
- Future scaling makes it worse, not better
  - More than 100 watts for latest Pentium

Design and Verification Problems



US005526514A

United States Patent [19]

Pradhan et al.

[11] Patent Number: 5,526,514

[45] Date of Patent: Jun. 11, 1996

[54] METHOD FOR CIRCUIT VERIFICATION AND MULTI-LEVEL CIRCUIT OPTIMIZATION BASED ON STRUCTURAL IMPLICATIONS

[76] Inventors: Dhiraj Pradhan, 1106 Langford St., College Station, Brazos County, Tex. 77840; Wolfgang Kunz, Heinersdorfer Str. 12 Stadtiel Lichterfelde, Berlin, Germany

[21] Appl. No.: 263,721

[22] Filed: Jun. 21, 1994

[51] Int. Cl.[6] G06F 3/00

[52] U.S. Cl. 395/500; 364/491; 371/67.1

[58] Field of Search 364/489, 490, 364/491; 395/500; 371/11.1, 11.2, 23, 27, 67.1, 71

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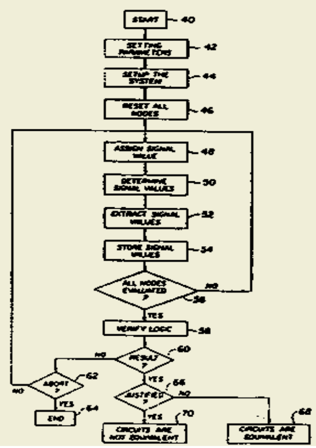
Primary Examiner—Kevin J. Teska
Assistant Examiner—Tan Nguyen
Attorney, Agent, or Firm—Harris, Tucker & Hardin

[57] ABSTRACT

A method for verifies that two integrated circuits are functionally equivalent by extracting equivalencies between internal nodes of the two circuits. Values are assigned to internal nodes in the first circuit and the effects of the assignments are determined in the rest of the first circuit and the second circuit. These effects, or implications, are analyzed to find internal equivalents between the first and second circuit. These steps are repeated with different values assigned to different nodes in the first circuit. The set of stored implications is used to determine if the two circuits are functionally equivalent.

A method is also disclosed for using the equivalencies, or indirect implications determined above to remove redundancies from the second circuit using a set of predetermined transformations. Based on an indirect implication a particular transform is selected and applied to the second circuit. This transformation is intended to create redundancies elsewhere in the circuit that can be removed thus optimizing the second circuit.

6 Claims, 3 Drawing Sheets



Non-exclusive licenses to Mentor Graphics and Motorola

For suitable licensing agreement please contact

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US Patent

Pradhan et al. Patent Number : 5,526,514

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METHOD FOR CIRCUIT VERIFICATION AND MULTI_LEVEL CIRCUIT OPTIMIZATION BASED ON STRUCTURAL IMPLICATIONS

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Dr. Pradhan 00-44-117-954 5637

Patent first rejected due to confusion over

Pradhan/Kunz instead of Kunz/Pradhan

A fundamentally new approach

Basis of the Equivalence Checker FormalPro introduced by Mentor Graphics in 2002.

www.mentor.com/formalpro

W. Kunz and D. Pradhan "Recursive Learning: A New Implication Technique for Efficient Solutions to CAD Problems" , IEEE Transactions on Computer-Aided Design; pp.1143-1158; Sept.,'94.

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THE FUTURE PROBLEM

THE SILICON BASED CMOS TECHNOLOGIES ARE PREDICTED TO REACH THEIR ULTIMATE LIMITS SHORTLY AFTER 2010

Nanotechnology (Introduction)

- Feature size nearing the physical limits
- Fabrication process approaching limits
- Power consumption – a concern
- Quantum effects need to be accounted for
- Solution? ***Nanotechnology***

What is Nanotechnology

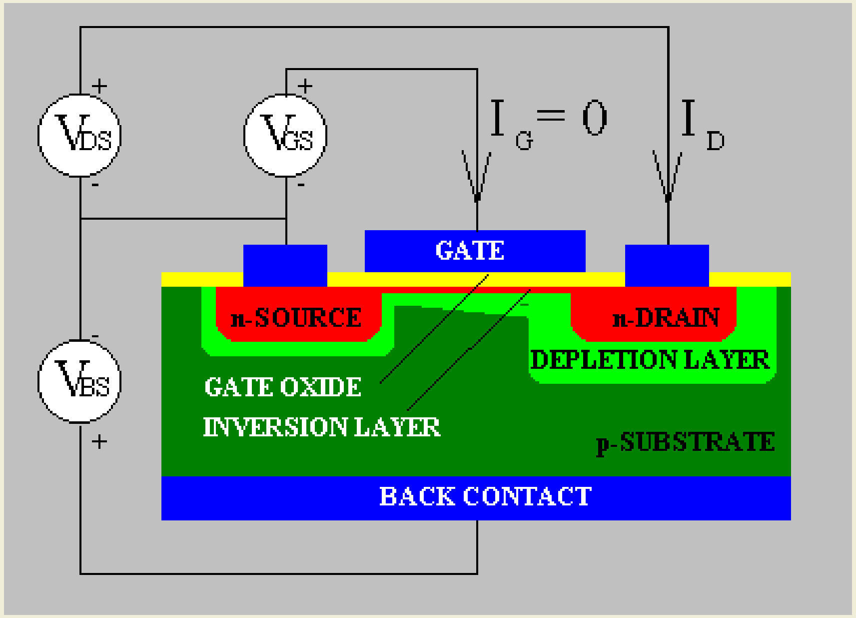
Many things to many people but two aspects are common

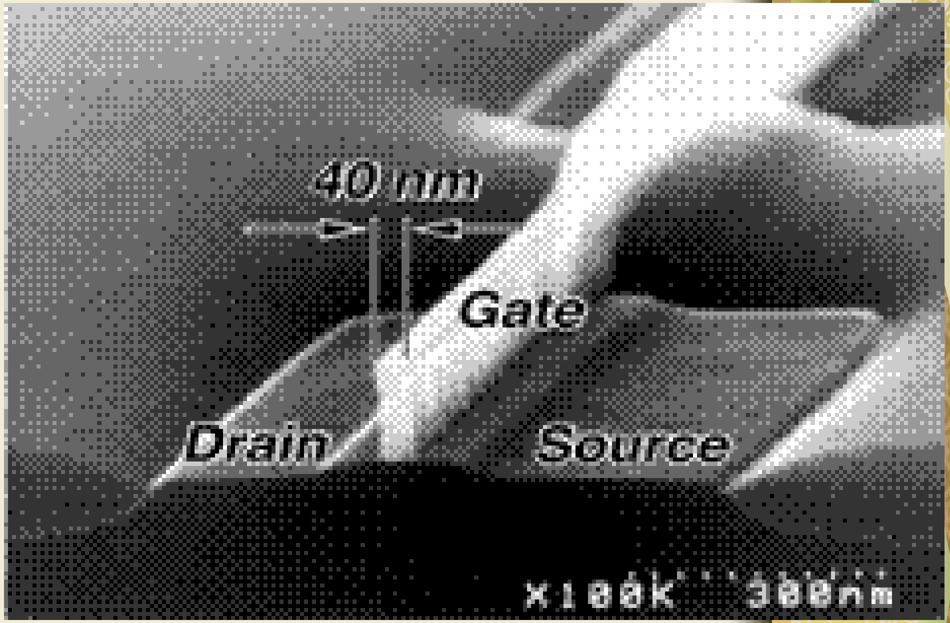
- Creation of "new" materials and devices from being able to manipulate properties at the levels of the atoms
- Exploitation of strange and new properties of materials of less than 100 nm such as nanopowders and nanocrystals

Myths of Nanotechnology

- Instant desktop assembly of cheese sandwiches from wood or waste
- Nanotechnology is midget submarines or robots (nanobots) that swim in the human bloodstream to repair people
- Nanotechnology will let people live forever
- Nanotechnology is about making things smaller
- Nanotechnology is the science fiction

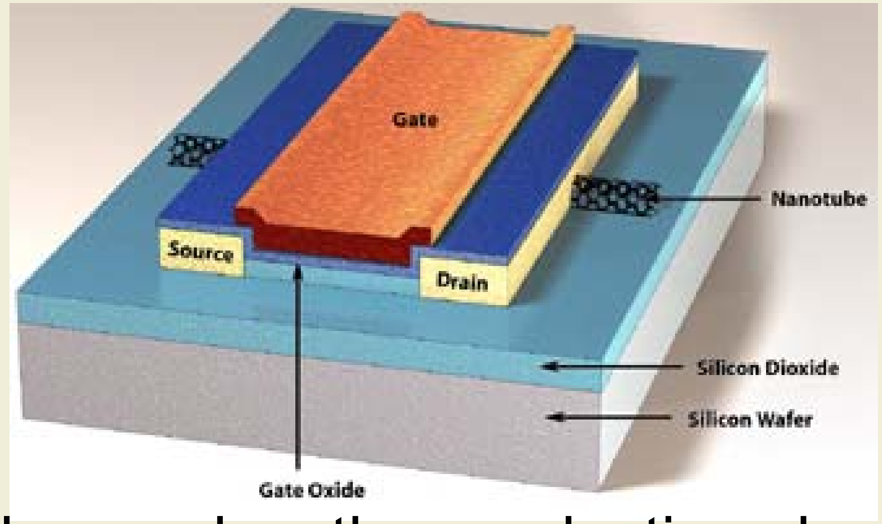
Nano-Scale MOSFET





- *Metal Oxide Semiconductor FET*
  - Half thickness of the gate is called “Feature size λ”
  - Current feature sizes in production – 90nm (Intel Pentium 5)
  - Demonstrated feature sizes up to 20nm (IBM).

Carbon Nanotube FET



- CNT can be used as the conducting channel of a MOSFET.
- All CNFETs are pFETs by nature.
- nFETs can be made through
  - **Annealing**
  - **Doping**
- Very low current and power consumption
- Although tubes are 3nm thick CNFETs are still the size of the contacts, about 20nm.

Future of Nanotechnology

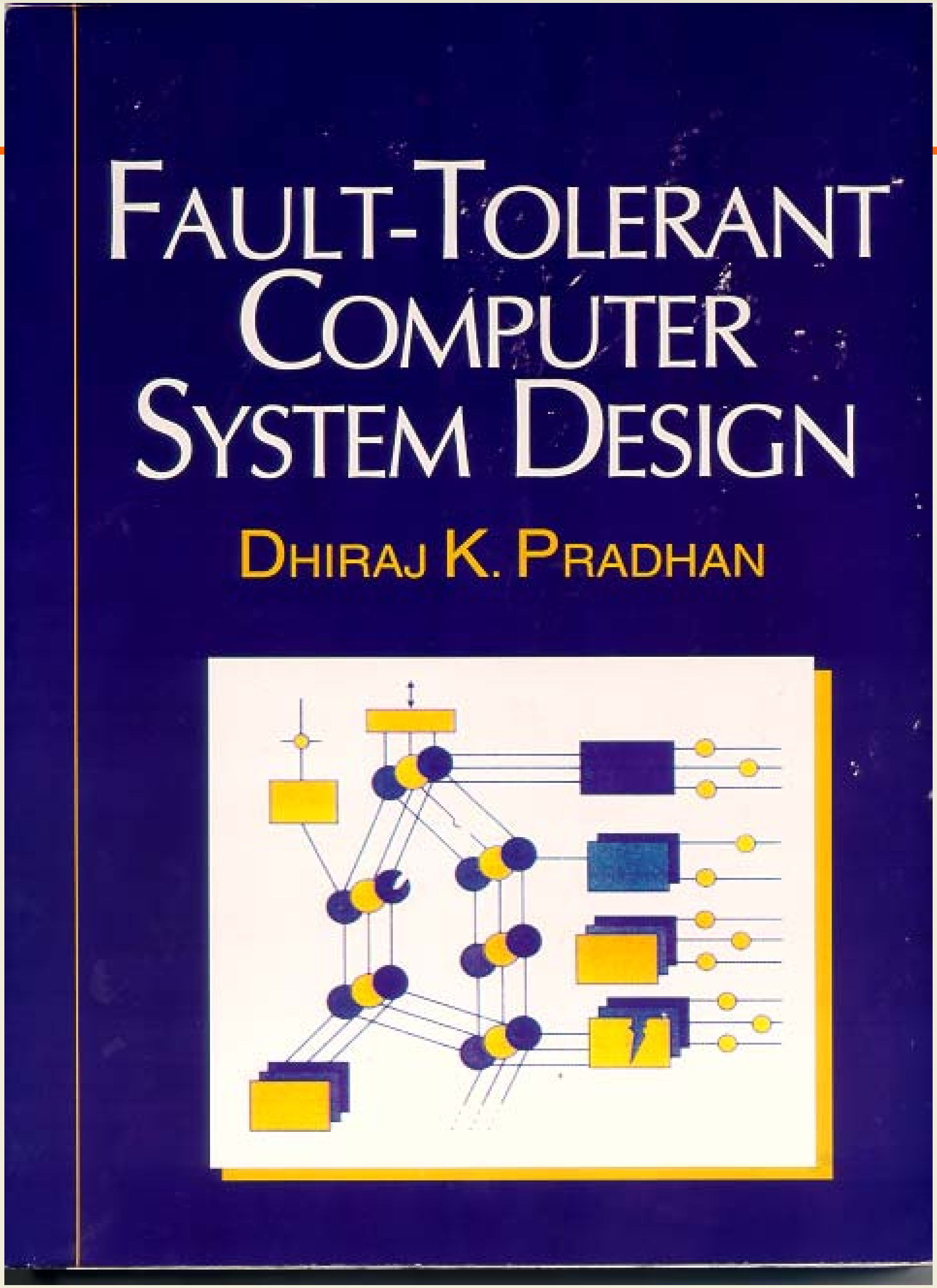
- High speed computing (Intel’s 10Ghz chip, 100 G flop proteomic analysis computer
- Sensors (chemical, biological and diagnostics)
- Self assembled materials, devices and systems

Open Problems and Initiatives

- Fabrication using DNA for self assembly (Technion-Israel; *Science*, Nov 2003)
- Memory array of nanotubes using junctions as bit storages (Lieber at Harvard)
- Using nanotube arrays to make computing elements (DeHon at Caltech)
- Fabricate FPGAs using CNFETs (Avouris at IBM)

Related Research at Bristol

- Enabling Technologies
- Defect Tolerance
  - Unreliable manufacturing
  - Self assembly
- Fault Tolerance
  - Fundamentals noise problems


FAULT-TOLERANT
COMPUTER
SYSTEM DESIGN
DHIRAJ K. PRADHAN